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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,674	03/18/2004	William F. Clark JR.	BUR920030158US1	2673

29154 7590 06/15/2005

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EXAMINER	
QUINTO, KEVIN V	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 06/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/708,674	CLARK ET AL.	
	Examiner	Art Unit	
	Kevin Quinto	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) *18-34* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claims 18-34 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on May 25, 2005.

Claim Objections

2. Claims 3, 9, and 14 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

3. Independent claims 1, 7, and 13 each describe a fin-type transistor having "fins extending from the substrate." However claims 3, 9, and 14 (dependent upon claims 1, 7, and 13 respectively) state that the fin-type transistor is a multiple fin transistor. Therefore claims 3, 9, and 14 are redundant.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Independent claims 1, 7, and 13 each describe a fin-type transistor having "fins extending from the substrate." However claims 3, 9, and 14 (dependent upon claims 1, 7, and 13 respectively) state that the fin-type transistor is a multiple fin transistor. It is unclear to the examiner as to whether or not independent claims 1, 7, and 13 describe a *plurality of fin transistors* OR *a multiple fin transistor*. Therefore the examiner has rejected claims 1-17 for both of these situations. The *plurality of fin transistors* interpretation of claims 1, 7, 13 and its dependent claims (claims 2, 4, 8, 10, and 15) are rejected under 35 U.S.C. 102 (e) with Chau et al. (USPN 6,858,478 B2). The remaining dependent claims (claims 3, 5, 6, 9, 11, 12, 14, 16, and 17) are rejected under 35 U.S.C. 103 (a) with Chau et al. (USPN 6,858,478 B2) combined with Hu et al. (USPN 6,413,802 B1) and Ahmed et al. (6,787,439 B2). The *multiple fin transistor* interpretation of claims 1, 7, 13 and its dependent claims (claims 2, 3, 4, 8, 9, 10, 14, and 15) are rejected under 35 U.S.C. 103 (a) with Chau (USPN 6,858,478 B2) and Hu et al. (USPN 6,413,802 B1). The remaining dependent claims (claims 5, 6, 11, 12, 16, and 17) are rejected under 35 U.S.C. 103 (a) with Chau et al. (USPN 6,858,478 B2) combined with Hu et al. (USPN 6,413,802 B1) and Ahmed et al. (6,787,439 B2). In this case, claims 3, 9, and 14 are also objected to since they do not further delimit independent claims 1, 7, and 13 respectively (see above section titled *Claim Objections*).

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1, 2, and 4 are rejected under 35 U.S.C. 102(e) as being anticipated by Chau et al. (USPN 6,858,478 B2).

9. So far as understood in claim 1, Chau et al. (USPN 6,858,478 B2, hereinafter referred to as the "Chau" reference) discloses a similar device. Figures 7A and 7B of Chau each disclose a fin-type field effect transistor with a fin (702) extending from a substrate (700). The fin (702) has a gate dielectric (712, 714) with different thicknesses. It is understood that a plurality of fins is formed on the substrate (700), each with a gate dielectric having different thicknesses.

10. So far as understood in claim 2, it is understood that a plurality of fins or transistors is formed on the substrate (700), each with the gate dielectric having different thicknesses. The examiner notes the limitation regarding the use of two different types of transistors with different gate dielectric thicknesses. However the examiner would like to point out that a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the

prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 370 F.2d 576, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 312 F.2d 937, 939, 136 USPQ 458, 459 (CCPA 1963). Therefore claim 2 is not patentable over the Chau reference.

11. So far as understood in claim 4, figure 7B of Chau shows that the gate dielectric has a greater thickness due to multiple layers (720, 722) while the smaller thickness is caused by less layers (720).

12. Claims 7, 8, and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Chau et al. (USPN 6,858,478 B2).

13. So far as understood in claim 7, Chau (USPN 6,858,478 B2) discloses a similar device. Figures 7A and 7B of Chau each disclose a fin-type field effect transistor with a fin (702) extending from a substrate (700). Each fin (702) comprises a channel region with source and drain regions (not shown) on opposite sides of the channel region. The fin (702) has a gate dielectric (712, 714) with different thicknesses which covers the channel region. It is understood that a plurality of fins is formed on the substrate (700), each with a gate dielectric having different thicknesses.

14. So far as understood in claim 8, it is understood that a plurality of fins or transistors is formed on the substrate (700), each with the gate dielectric having different thicknesses. The examiner notes the limitation regarding the use of two different types of transistors with different gate dielectric thicknesses. However the

examiner would like to point out that a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art.. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 370 F.2d 576, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 312 F.2d 937, 939, 136 USPQ 458, 459 (CCPA 1963). Therefore claim 2 is not patentable over the Chau reference.

15. So far as understood in claim 10, figure 7B of Chau shows that the gate dielectric has a greater thickness due to multiple layers (720, 722) while the smaller thickness is caused by less layers (720).

16. Claims 13 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Chau et al. (USPN 6,858,478 B2).

17. So far as understood in claim 13, Chau (USPN 6,858,478 B2) discloses a similar device. Figures 7A and 7B of Chau each disclose a fin-type field effect transistor with a fin (702) extending from a substrate (700). The fin (702) has a gate dielectric (712, 714) with different thicknesses. It is understood that a plurality of fins or transistors is formed on the substrate (700), each with the gate dielectric having different thicknesses. The examiner notes the limitation regarding the use of two different types of transistors with different gate dielectric thicknesses. However the examiner would like to point out that a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably

distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 370 F.2d 576, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 312 F.2d 937, 939, 136 USPQ 458, 459 (CCPA 1963). Therefore claim 2 is not patentable over the Chau reference.

18. So far as understood in claim 15, figure 7B of Chau shows that the gate dielectric has a greater thickness due to multiple layers (720, 722) while the smaller thickness is caused by less layers (720).

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claims 3, 9, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chau et al. (USPN 6,858,478 B2) in view of Hu et al. (USPN 6,413,802 B1).

21. So far as understood in claim 3, Chau does not disclose the use of multiple fins in the fin type transistor. However the use of multiple fins in a fin type transistor is well known in the art. Hu et al. (USPN 6,413,802 B1, hereinafter referred to as the "Hu" reference) discloses that the use of multiple fins in a fin type transistor (figures 4 and 5 of Hu) has the benefit of reducing mobility degradation (column 2, lines 31-40) which is

a known problem in the art (column 1, lines 61-65). In view of Hu, it would therefore be obvious to implement multiple fins in the device of Chau.

22. So far as understood in claim 9, Chau does not disclose the use of multiple fins in the fin type transistor. However the use of multiple fins in a fin type transistor is well known in the art. Hu (USPN 6,413,802 B1) discloses that the use of multiple fins in a fin type transistor (figures 4 and 5 of Hu) has the benefit of reducing mobility degradation (column 2, lines 31-40) which is a known problem in the art (column 1, lines 61-65). In view of Hu, it would therefore be obvious to implement multiple fins in the device of Chau.

23. So far as understood in claim 14, Chau does not disclose the use of multiple fins in the fin type transistor. However the use of multiple fins in a fin type transistor is well known in the art. Hu (USPN 6,413,802 B1) discloses that the use of multiple fins in a fin type transistor (figures 4 and 5 of Hu) has the benefit of reducing mobility degradation (column 2, lines 31-40) which is a known problem in the art (column 1, lines 61-65). In view of Hu, it would therefore be obvious to implement multiple fins in the device of Chau.

24. Claims 5, 6, 11, 12, 16, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chau et al. (USPN 6,858,478 B2) in view of Ahmed et al. (USPN 6,787,439 B2).

25. So far as understood in claim 5, Chau does not disclose the use of cap layer over the fin. However the use of cap layers in a fin-type transistor is well known in the art. Ahmed et al. (USPN 6,787,439 B2, hereinafter referred to as the "Ahmed" reference)

discloses that the use of a silicon nitride cap layer has the benefit of protecting the fin during subsequent etch processes (column 3, lines 42-45). In view of Ahmed, it would therefore be obvious to use a cap layer in the device of Chau.

26. So far as understood in claim 6, the cap layer of Ahmed is made of silicon nitride (column 3, lines 42-45) while Chau uses films other than silicon nitride such as silicon dioxide, silicon oxynitride, tantalum pentaoxide, titanium oxide, hafnium oxide, zirconium oxide, aluminum oxide, silicates, PZT, and BST for the gate dielectric (column 14, lines 2-28); thus meeting the limitation of the claim.

27. So far as understood in claim 11, Chau does not disclose the use of cap layer over the fins. However the use of cap layers in a fin-type transistor is well known in the art. Ahmed (USPN 6,787,439 B2) discloses that the use of a silicon nitride cap layer has the benefit of protecting the fin during subsequent etch processes (column 3, lines 42-45). In view of Ahmed, it would therefore be obvious to use a cap layer in the device of Chau.

28. So far as understood in claim 12, the cap layer of Ahmed is made of silicon nitride (column 3, lines 42-45) while Chau uses films other than silicon nitride such as silicon dioxide, silicon oxynitride, tantalum pentaoxide, titanium oxide, hafnium oxide, zirconium oxide, aluminum oxide, silicates, PZT, and BST for the gate dielectric (column 14, lines 2-28); thus meeting the limitation of the claim.

29. So far as understood in claim 16, Chau does not disclose the use of cap layer over the fins. However the use of cap layers in a fin-type transistor is well known in the art. Ahmed (USPN 6,787,439 B2) discloses that the use of a silicon nitride cap layer

has the benefit of protecting the fin during subsequent etch processes (column 3, lines 42-45). In view of Ahmed, it would therefore be obvious to use a cap layer in the device of Chau.

30. So far as understood in claim 17, the cap layer of Ahmed is made of silicon nitride (column 3, lines 42-45) while Chau uses films other than silicon nitride such as silicon dioxide, silicon oxynitride, tantalum pentaoxide, titanium oxide, hafnium oxide, zirconium oxide, aluminum oxide, silicates, PZT, and BST for the gate dielectric (column 14, lines 2-28); thus meeting the limitation of the claim.

31. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chau et al. (USPN 6,858,478 B2) in view of Hu et al. (USPN 6,413,802 B1).

32. So far as understood in claims 1 and 3, Chau (USPN 6,858,478 B2) discloses a similar device. Figures 7A and 7B of Chau each disclose a fin-type field effect transistor with a fin (702) extending from a substrate (700). The fin (702) has a gate dielectric (712, 714) with different thicknesses. Chau does not disclose the use of multiple fins in the fin type transistor. However the use of multiple fins in a fin type transistor is well known in the art. Hu (USPN 6,413,802 B1) discloses that the use of multiple fins in a fin type transistor (figures 4 and 5 of Hu) has the benefit of reducing mobility degradation (column 2, lines 31-40) which is a known problem in the art (column 1, lines 61-65). In view of Hu, it would therefore be obvious to implement multiple fins in the device of Chau.

33. So far as understood in claim 2, the examiner notes the limitation regarding the use of two different types of transistors with different gate dielectric thicknesses.

However the examiner would like to point out that a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 370 F.2d 576, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 312 F.2d 937, 939, 136 USPQ 458, 459 (CCPA 1963). Therefore claim 2 is not patentable over the Chau reference.

34. So far as understood in claim 4, figure 7B of Chau shows that the gate dielectric has a greater thickness due to multiple layers (720, 722) while the smaller thickness is caused by less layers (720).

35. Claims 7, 8, 9, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chau et al. (USPN 6,858,478 B2) in view of Hu et al. (USPN 6,413,802 B1).

36. So far as understood in claims 7 and 9, Chau (USPN 6,858,478 B2) discloses a similar device. Figures 7A and 7B of Chau each disclose a fin-type field effect transistor with a fin (702) extending from a substrate (700). Each fin (702) comprises a channel region with source and drain regions (not shown) on opposite sides of the channel region. The fin (702) has a gate dielectric (712, 714) with different thicknesses which covers the channel region. Chau does not disclose the use of multiple fins in the fin type transistor. However the use of multiple fins in a fin type transistor is well known in the art. Hu (USPN 6,413,802 B1) discloses that the use of multiple fins in a fin type

transistor (figures 4 and 5 of Hu) has the benefit of reducing mobility degradation (column 2, lines 31-40) which is a known problem in the art (column 1, lines 61-65). In view of Hu, it would therefore be obvious to implement multiple fins in the device of Chau.

37. So far as understood in claim 8, the examiner notes the limitation regarding the use of two different types of transistors with different gate dielectric thicknesses. However the examiner would like to point out that a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 370 F.2d 576, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 312 F.2d 937, 939, 136 USPQ 458, 459 (CCPA 1963). Therefore claim 2 is not patentable over the Chau reference.

38. So far as understood in claim 10, figure 7B of Chau shows that the gate dielectric has a greater thickness due to multiple layers (720, 722) while the smaller thickness is caused by less layers (720).

39. Claims 13, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chau et al. (USPN 6,858,478 B2) in view of Hu et al. (USPN 6,413,802 B1).

40. So far as understood in claims 13 and 14, Chau (USPN 6,858,478 B2) discloses a similar device. Figures 7A and 7B of Chau each disclose a fin-type field effect

transistor with a fin (702) extending from a substrate (700). The fin (702) has a gate dielectric (712, 714) with different thicknesses. Chau does not disclose the use of multiple fins in the fin type transistor. However the use of multiple fins in a fin type transistor is well known in the art. Hu (USPN 6,413,802 B1) discloses that the use of multiple fins in a fin type transistor (figures 4 and 5 of Hu) has the benefit of reducing mobility degradation (column 2, lines 31-40) which is a known problem in the art (column 1, lines 61-65). In view of Hu, it would therefore be obvious to implement multiple fins in the device of Chau. The examiner notes the limitation regarding the use of two different types of transistors with different gate dielectric thicknesses. However the examiner would like to point out that a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 370 F.2d 576, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 312 F.2d 937, 939, 136 USPQ 458, 459 (CCPA 1963). Therefore claim 2 is not patentable over the Chau reference.

41. So far as understood in claim 15, figure 7B of Chau shows that the gate dielectric has a greater thickness due to multiple layers (720, 722) while the smaller thickness is caused by less layers (720).

42. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chau et al. (USPN 6,858,478 B2) in view of Hu et al. (USPN 6,413,802 B1) as applied to claim 1 above and further in view of Ahmed et al. (USPN 6,787,439 B2).

43. So far as understood in claim 5, Chau does not disclose the use of cap layer over the fin. However the use of cap layers in a fin-type transistor is well known in the art. Ahmed (USPN 6,787,439 B2) discloses that the use of a silicon nitride cap layer has the benefit of protecting the fin during subsequent etch processes (column 3, lines 42-45). In view of Ahmed, it would therefore be obvious to use a cap layer in the device of Chau.

44. So far as understood in claim 6, the cap layer of Ahmed is made of silicon nitride (column 3, lines 42-45) while Chau uses films other than silicon nitride such as silicon dioxide, silicon oxynitride, tantalum pentaoxide, titanium oxide, hafnium oxide, zirconium oxide, aluminum oxide, silicates, PZT, and BST for the gate dielectric (column 14, lines 2-28); thus meeting the limitation of the claim.

45. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chau et al. (USPN 6,858,478 B2) in view of Hu et al. (USPN 6,413,802 B1) as applied to claim 7 above and further in view of Ahmed et al. (USPN 6,787,439 B2).

46. So far as understood in claim 11, Chau does not disclose the use of cap layer over the fins. However the use of cap layers in a fin-type transistor is well known in the art. Ahmed (USPN 6,787,439 B2) discloses that the use of a silicon nitride cap layer has the benefit of protecting the fin during subsequent etch processes (column 3, lines

42-45). In view of Ahmed, it would therefore be obvious to use a cap layer in the device of Chau.

47. So far as understood in claim 12, the cap layer of Ahmed is made of silicon nitride (column 3, lines 42-45) while Chau uses films other than silicon nitride such as silicon dioxide, silicon oxynitride, tantalum pentaoxide, titanium oxide, hafnium oxide, zirconium oxide, aluminum oxide, silicates, PZT, and BST for the gate dielectric (column 14, lines 2-28); thus meeting the limitation of the claim.

48. Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chau et al. (USPN 6,858,478 B2) in view of Hu et al. (USPN 6,413,802 B1) as applied to claim 14 above and further in view of Ahmed et al. (USPN 6,787,439 B2).

49. So far as understood in claim 16, Chau does not disclose the use of cap layer over the fins. However the use of cap layers in a fin-type transistor is well known in the art. Ahmed (USPN 6,787,439 B2) discloses that the use of a silicon nitride cap layer has the benefit of protecting the fin during subsequent etch processes (column 3, lines 42-45). In view of Ahmed, it would therefore be obvious to use a cap layer in the device of Chau.

50. So far as understood in claim 17, the cap layer of Ahmed is made of silicon nitride (column 3, lines 42-45) while Chau uses films other than silicon nitride such as silicon dioxide, silicon oxynitride, tantalum pentaoxide, titanium oxide, hafnium oxide, zirconium oxide, aluminum oxide, silicates, PZT, and BST for the gate dielectric (column 14, lines 2-28); thus meeting the limitation of the claim.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KVQ

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